REMARKS

A. Background

Claims 50, 51, 53, 56, 77, 78, 80-82, and 96 were pending in the application at the time of the Office Action. All of the pending claims were rejected as being obvious over cited art. By this response applicant has not cancelled or amended any pending claim or added any new claims. As such, Applicant requests the Examiner's reconsideration of claims 50, 51, 53, 56, 77, 78, 80-82, and 96 in light of the following remarks.

B. Rejection Based on 35 USC § 103

Pages 2-9 of the Office Action reject claims 50, 51, 53, 56, 77, 78, 80-82, 85-89, and 96 under 35 USC § 103(a) as being unpatentable over U.S. Publication No. 2002/0195619 to Makimoto ("*Makimoto*") in view of U.S. Patent No. 6,392,262 to Shiraishi ("*Shiraishi*"), and further in view of a paper entitled *Low-Resistance Nonalloyed Ohmic Contact to p-type GaN Using Strained InGaN Contact Layer* by Kumakura et al ("*Kumakura*"). Applicant respectfully traverses this rejection. Of the rejected claims, claims 50 and 81 are independent claims.

The Office Action asserts that the nitride semiconductor structure disclosed in *Makimoto* includes many of the limitations recited in independent claims 50 and 81, but concedes that *Makimoto* fails to teach "an indium-containing p-type nitride semiconductor layer formed directly on a second portion of said top surface of said p-type base layer, wherein said n-type emitter layer is not formed on the second portion, and said indium-containing p-type nitride semiconductor layer ... does not contact said n-type emitter layer," as recited in claims 50 and 81. The Office Action then cites to *Shiraishi* to attempt to remedy this deficiency of *Makimoto*, asserting that *Shiraishi* "discloses a similar nitride semiconductor structure (fig. 6)" that includes the limitations not found in *Makimoto*. In particular, the Office Action asserts that *Shiraishi* contains "an indium-containing p-type nitride semiconductor layer (6)" that reads on the claimed "indium-containing p-type nitride semiconductor layer." The Office Action alleges that it would have been obvious to "combine the structure of *Shiraishi* in the teaching of *Makimoto*" to arrive at the inventions recited in claims 50 and 81 to produce "a highly reliable and well reproducible hetero-junction bipolar transistor." Applicant respectfully disagrees and submits that the Office Action has mischaracterized the teachings of *Shiraishi*.

As noted above, the Office Action has asserted that *Shiraishi* discloses a nitride semiconductor structure having a p-type nitride semiconductor layer 6. However, Applicant submits that both of these assertions are incorrect. *Shiraishi* discloses that the purpose for the *Shiraishi* invention is to overcome various problems that occur while using GaAs layers (i.e., in an arsenide structure). See col. 1, line 15 through col. 3, line 4. As such, *Shiraishi* discloses a hetero-junction bipolar transistor that is fabricated on a GaAs substrate 1 and that uses GaAs layers. See, e.g., col. 4, lines 3-50; and col. 8, lines 20-32. In fact, all of the layers disclosed in the various embodiments, including layer 6 cited in the Office Action, are based on GaAs or a compound that includes GaAs, such as InGaAs or AlGaAs. Significantly, none of the layers disclosed in *Shiraishi* are based on a nitride structure. As such, contrary to the assertion of the Office Action, *Shiraishi* does not disclose a nitride semiconductor structure. Furthermore, while *Shiraishi* discloses layer 6 as being a p-type layer, *Shiraishi* only discloses that layer 6 is comprised of InGaAs, making layer 6 decidedly not a nitride layer. See col. 8, line 39.

In contrast to *Shiraishi*, the *Makimoto* semiconductor structure is a nitride semiconductor structure based on a nitride structure. Thus, while *Makimoto* is directed to a nitride semiconductor structure, *Shiraishi* is directed to an arsenide structure. This is significant in that one would not look to *Shiraishi*'s arsenide structure to modify the *Makimoto* nitride structure. Both types of structure have their own unique challenges and design considerations. As such, it is not at all clear that any combination of *Makimoto* and *Shiraishi* would produce "a highly reliable and well reproducible hetero-junction bipolar transistor," contrary to the assertion of the Office Action.

Furthermore, even if, arguendo, one was to add the p-type layer 6 of *Shiraishi* to the *Makimoto* device in the allegedly obvious manner set forth in the Office Action, the resulting combination would not include all of the limitations recited in the rejected claims. Specifically, because layer 6 of *Shiraishi* is disclosed as an InGaAs layer, the resulting combination would not teach or suggest "an indium-containing p-type nitride semiconductor layer," as recited in rejected claims 50 and 81.

In light of the above, Applicant respectfully submits that a *prima facie* case of obviousness has not been established regarding claims 50 and 81. Accordingly, Applicant respectfully requests that the obviousness rejection with respect to claims 50 and 81 be withdrawn.

Claims 51, 53, 56, 77, 78, 80, 82, 85-89, and 96 variously depend from claims 50 and 81 and thus incorporate the limitations thereof. As such, applicant submits that claims 51, 53, 56, 77, 78, 80, 82, 85-89, and 96 are distinguished over the cited art for at least the same reasons as discussed above with regard to claims 50 and 81. Accordingly, Applicant respectfully requests that the obviousness rejection with respect to claims 51, 53, 56, 77, 78, 80, 82, 85-89, and 96 also be withdrawn.

No other objections or rejections are set forth in the Office Action.

C. Conclusion

Applicant notes that this response does not discuss every reason why the claims of the present application are distinguished over the cited art. Most notably, applicant submits that many if not all of the dependent claims are independently distinguishable over the cited art. Applicant has merely submitted those arguments which it considers sufficient to clearly distinguish the claims over the cited art.

In view of the foregoing, applicant respectfully requests the Examiner's reconsideration and allowance of claims 50, 51, 53, 56, 77, 78, 80-82, 85-89, and 96.

The Commissioner is hereby authorized to charge payment of any of the following fees that may be applicable to this communication, or credit any overpayment, to Deposit Account No. 23-3178: (1) any filing fees required under 37 CFR § 1.16; (2) any patent application and reexamination processing fees under 37 CFR § 1.17; and/or (3) any post issuance fees under 37 CFR § 1.20. In addition, if any additional extension of time is required, which has not otherwise been requested, please consider this a petition therefor and charge any additional fees that may be required to Deposit Account No. 23-3178.

In the event there remains any impediment to allowance of the claims which could be clarified in a telephonic interview, the Examiner is respectfully requested to initiate such an interview with the undersigned.

Dated this 26th day of August 2009.

Respectfully submitted,

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